IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, v. STMICROELECTRONICS N.V., STMICROELECTRONICS INTERNATIONAL N.V., and STMICROELECTRONICS, INC, Defendants.	CIVIL ACTION NO. 6:21-CV-00727-ADA JURY TRIAL DEMANDED

PLAINTIFF'S SURREPLY CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Purdue's constructions are consistent with the claim language, the specification, and the prosecution history of the Asserted Patents. In contrast, ST's constructions and arguments should be rejected because they are contrary to positions ST has taken in its IPRs regarding the same patents, attempt to inject improper limitations into the claims, and completely disregard established law and principles.[1]

II. DISPUTED CLAIM CONSTRUCTIONS

A. '112 Patent

1. "a second, thicker oxide layer over said top surface and sidewall of each of said first gate"/ "a gate oxide layer thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates": Claims 1 and 6

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate"	"an oxidation layer formed, created, or grown by reacting the gate, thicker than the first oxide layer"/ "an oxidation layer formed, created or grown by reacting the gate"

Contrary to ST's contention, its proposed construction does not provide any structural characteristic. Indeed, ST admits that its construction is "based on ***formation***" (Dkt. 74 at 1), and thus, improperly introduces a method step into an apparatus claim. (Emphasis added).

Unlike "dry-aged steak" or "forged steel," both of which relate to very particular and well-understood techniques, the '112 Patent expressly provides that the fabrication of the claimed product "can be accomplished ***in a variety of ways*** well known in the art." '112 Patent at 5:34-46

[1]Since the USPTO adopted the claim construction standard used in district courts for proceedings before the PTAB in October 2018, ST's reliance on *GoPro, Inc. v. C&A Mktg., Inc.*, No. 16-CV-03590-JST, 2017 WL 3131449 (N.D. Cal. July 24, 2017) is misplaced. ST's IPR petitions ***are relevant*** to the proper construction of the disputed terms, and its inconsistent positions is telling. *Guardant Health, Inc. v. Found. Med., Inc.*, No. CV 17-1616-LPS-CJB, 2019 WL 5677748, at *8 (D. Del. Nov. 1, 2019), *report and recommendation adopted*, No. CV 17-1616-LPS-CJB, 2020 WL 1329513 (D. Del. Mar. 23, 2020). And irrespective of the grounds for patent invalidation in IPRs, ST and its expert clearly understood and applied the term it now alleges is indefinite to the prior art.

("***The method set forth in Appendix I (through step "m") and Appendix II (through step 15 and into step 16) represents one method***, with some alternative processing steps, for fabricating the intermediate semiconductor product 58 of FIG. 5.") (emphasis added). Despite this unambiguous language, ST claims that the specification "disavows" any alternatives to its proposed method, i.e., "formed, created or grown by reacting the gate." Dkt. 74 at 1. But disavowal of claim scope must be ***clear and unmistakable***, which is not the case here. *See Continental Circuits LLC v. Intel Corporation*, No. 2018-1076 (Fed. Cir. Feb. 8, 2019) (holding that "the district court erred in limiting the claims to require a repeated desmear process" as it improperly imported a limitation from the specification into the claims). Like in *Continental*, the plain language of the claims does not recite ST's process, and the specification makes clear that the described process is just one method of making one embodiment, without any limitation. '112 Patent at 5:34-46.

Moreover, in *Continental*, even though "the specification not only 'repeatedly distinguishe[d] the process covered by the patent from the prior art and its use of a 'single desmear process,'' but also characterized 'the present invention' as using a repeated desmear process," the Federal Circuit concluded that none of these statements rose to the level of a clear and unmistakable disclaimer. In contrast, ST points solely to and heavily relies on the "so long as" language that appears only ***once*** in the entire patent. Dkt. 74 at 1, 3; *see generally* '112 Patent (confirming same). This alone is insufficient to meet the exacting standard in light of the claim language, the specification, and the knowledge of those skilled in the art. *See, e.g.*, '112 Patent at 3:2-7 ("[N]o limitation of the scope of the invention is… intended, and that alterations and further modifications in the illustrated device and further applications of the principles of the invention as illustrated therein are contemplated as would normally occur to one skilled in the art."); *id*. at 8:14-

20 (stating the description "is to be considered as illustrative and not restrictive in character");[2] Declaration of Dr. Ishwara Bhat ("Bhat Decl."), ¶ 12 (stating that the oxide layer could be made using "growth or deposition processes").

ST's reliance on the Baliga textbook is also misplaced because it is based on a complete mischaracterization the following portion of the '112 Patent:

> ***Several different types of vertical power MOSFETs have been proposed, including the double-diffused MOSFET (DMOSFET) and the trench-gate or UMOSFET. These and other power MOSFETs*** are described in a textbook by B. Jayant Baliga entitled Power Semiconductor Devices, PWS Publishing Co. (1996), the disclosure of, which is hereby incorporated herein by reference.

'112 Patent at 1:42-49 (emphasis added). As is evident from the actual language in the specification, nothing in this section concerns making the oxide layers at issue, fabrication of a MOSFET, the conventional process, or even deposited oxide. Instead, the '112 Patent disclosure and incorporation of the Baliga textbook relate solely to the products, i.e., the different types of MOSFETs, and not any process. Hence, ST's discussion and emphasis on the conventional process described in the cited two-pages of the Baliga textbook is wholly irrelevant.

Because the claim language itself is purely structural and does not recite any adjective in the form of a verb plus "ed" that suggests any method whatsoever, like "dry-aged steak" or "forged steel, ST's construction must be rejected.

[2] In its criticisms of Purdue for some alleged inconsistency, ST readily admits to "import[ing] from the specification a limitation (i.e., an oxidation layer that is grown as opposed to deposited)" into the asserted claims, despite express language prohibiting such restriction. The inconsistency lies with ST's claim construction positions. For example, with respect to the '633 Patent, ST's expert relies on non-limiting language to argue that Claim 9 relates to "other types of devices," but ST disregards such language here for the '112 Patent.

B. '633 Patent

1. "double-implanted metal-oxide semiconductor field-effect transistor": Claim 9

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"The preamble is not limiting"	"The preamble is limiting"

The preamble is not limiting because it merely provides context for and a descriptive name to the set of limitations, such as silicon-carbide substrate and the JFET-region. ST does not contend that the preamble to Claim 9 is necessary to provide antecedent basis or that the applicant placed clear reliance on the preamble during prosecution for patentability. *See generally*, Dkt. 74 at 5-6; Dkt. 66 at 14-15.

More importantly, ST concedes that a POSITA would understand that Claim 9 is directed to a ***double-implanted*** semiconductor device based on the claim elements, without the preamble. *See* Dkt. 74 at 5-6; *see also* Dkt. 70-1, ¶ 13. Claim specifically recites (1) "a ***plurality of first base contact regions*** defined in the first source region, each of the ***plurality of first base contact regions*** being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode" and (2) "a ***plurality of second base contact regions*** defined in the second source region, each of the ***plurality of second base contact regions*** being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode." '633 Patent, Claim 9 (Emphasis added). Here, the second implant is the plurality of the base contact regions defined in the first implant which is the source region. Because the claim language itself describes what is "double implanted" according to the invention, so there is no need to implicitly add any further limitations via the preamble. Thus, at a minimum, "double-implanted" is not limiting.

The fact that ST and its expert rely on the specification to argue that the claim "could be read on other types of transistors" is also telling. Dkt. 74 at 5 (citing Subramanian Opening Decl.

¶¶ 34–35). Notably, paragraph 34 of Dr. Subramanian's Opening Declaration and the cited portions of the specification relate only to ***MOSFET*** devices and not just any other type of transistor. *See* Dkt. 66-1, ¶ 34; *see also* '633 Patent at 2: 26-27 ("The MOSFET may be a double-implanted MOSFET (DMOSFET). For example, the MOSFET may be a vertical DMOSFET"); *id*. 4:6-11 (Illustratively, the semiconductor device 10 is a vertical double-implanted metal-oxide semiconductor field-effect transistor (DMOSFET). However, in other embodiments, the semiconductor device 10 may be embodied as ***other types of MOSFET devices***.") (emphasis added).

Interestingly, ST contends that Purdue's reliance on the specification proves ST's point, i.e., the preamble is limiting. But ST does the same thing here by relying on the specification to argue that "the claim could be read on other types of transistors." Dkt. 74 at 5. Either the claims must be read in view of the specification, as both parties suggest, or in isolation, as ST urges in arguing that the preamble is limiting. ST cannot have it both ways.

2. "less than about three micrometers": Claim 9

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, no construction necessary.	Indefinite

ST has failed to prove that this term is indefinite by clear and convincing evidence. First, as discussed below, Dr. Subramanian does not qualify as a POSITA in this case. ST, therefore, relies on unsubstantiated attorney arguments devoid of any support, which is insufficient. *Twist, Inc. v. B GSE Grp., LLC*, No. 319CV00583MOCDSC, 2021 WL 2210892, at *8 (W.D.N.C. June 1, 2021) ("Without evidence from a POSITA, the Court cannot conclude [a] claim is indefinite."). Purdue, on the other hand, cites intrinsic and extrinsic evidence supporting its proposed constructions, including expert testimony, all of which firmly establish that this term is not indefinite and needs no construction.

Second, ST does not challenge the fact that terms of approximation like "about" or "at least about" are ubiquitous in patent claims, well-understood, and do not render patent claims indefinite. Thus, "less than about" here means "less than approximately."

Third, ST's boundary arguments lack merit. With respect to the upper boundary, and as explained in Purdue's responsive brief, both the asserted claim and the specification provide that it is "about" three (3) micrometers. '633 Patent, Claim 9; *id*. at 1:65-67; *id*. at 2:47-48; *id*. at 6:24-26. And contrary to ST's assertions, the specification clearly states that the JFET width is optimized according to two objectives: decreasing on-resistance and reducing the electric field in the oxide above the JFET region. *Id*. at 6: 6:21-27; *id*. at 6:45-50. A POSITA would also understand that other objectives for SiC JFET-region design include ensuring good forward current conduction and withstanding reverse blocking voltage. Bhat. Decl., ¶ 16.

With respect to the lower boundary, the specification provides an example: "about" one (1) micrometer. '633 Patent, Claim 9; *id*. at 1:66-67; *id*. at 2:48-49; *id*. at 3:26; *id*. at 6:26-27. More importantly, a POSITA would know that the JFET width ***cannot*** be arbitrarily reduced to an infinitesimal dimension, such as 0.001micrometer or 0.0001 micrometers (0.0001micrometers is less than half the size of a single silicon atom, which measures 0.00024 micrometers), or to zero (in which case the device could not be a DMOSFET at all), as ST suggests. Bhat. Decl., ¶ 18; *see also id*., 19 (explaining the lower end for the JFET width cannot go below 0.6 micrometers).

Finally, a variation of ±10% during manufacturing is expected when numerical values are used for the JFET regions of SiC DMOSFETs. *Id*., ¶¶ 13-14. Again, a POSITA would understand this. Despite ST's contention, this variation is well-understood in the field. *See, e.g., id.,* ¶ 14 (citing Wolf and Tauber, *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (2000)" at p. 533 (referencing the 10% tolerance for polysilicon lithography and etching, which applies to

polysilicon used on both SiC and silicon wafers). As Dr. Bhat explains, this variation is expected for tolerances in the lithography and etching in a typical manufacturing facility and may depend on other facility specific factors. *Id*., ¶ 15.

III. REQUEST TO EXCLUDE DR. SUBRAMANIAN

Purdue's request is proper. *See, e.g., Merck & Co. v. Teva Pharms. USA, Inc*., 347 F.3d 1367, 1372 (Fed. Cir. 2003) (ruling district court properly discounted accused infringer's expert's testimony on claim construction issue due to lack of experience, and therefore did not present evidence of how one of skill in the relevant art would understand the claim terms). Here, Dr. Subramanian's opinions should be excluded or give little to no weight because he lacks the relevant qualifications. *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1362 (Fed. Cir. 2008) ("Admitting testimony from a person…with no skill in the pertinent art, serves only to cause mischief and confuse the factfinder.").

Although ST and Dr. Subramanian assert that he has "researched and published numerous papers on wide bandgap devices for more than a decade," neither could identify or point to even a single publication. Dkt. 74 at 10; Dkt. 74-1, ¶ 5. And nowhere in the two declarations submitted in support of ST's arguments does Dr. Subramanian claim to have ***any*** experience with SiC semiconductor devices. *See* Dkt. 74-1; Dkt. 66-1; *see also* Dkt. 70-12 (confirming Dr. Subramanian has no patents, publications, or presentations involving SiC power semiconductor devices).

ST's reliance on *Hologic, Inc. v. Minerva Surgical, Inc*., 764 F. App'x 873 (Fed. Cir. 2019) is also misplaced. In *Hologic*, the patent at issue "explicitly disclose[d] that the invention is applicable to ***body cavities generally*** and indicate[d] that ***the problem with perforations is not unique to the ablation of the uterus***." *Id*. at 876 (emphases added); *see also id*. at 875 (stating that the patent describes "a system and method that pressurizes a body cavity and detects whether the

body cavity can maintain a pressurized condition."). Here, in contrast, the claimed inventions relate to high-voltage semiconductor devices, the specifications repeatedly refer to SiC, and the claims at issue for all disputed terms are specifically directed to SiC devices. *See, e.g.*, '112 Patent at 2:24-26 ("The present invention provides high voltage power MOSFETs, with self-aligned source contacts and a method for making the same"); *id*. at 1:50-60 (detailing the advantages of SiC devices); '633 Patent at 1:12-15 ("The present disclosure relates … more particularly to semiconductor devices for high-voltage power applications."); '112 Patent, Claim 1 ("A silicon carbide power MOSFET, comprising…"), Claim 6 ("MOSFET structure, comprising: a silicon carbide wafer…"); '633 Patent, Claim 9 ("A double-implanted metal-oxide semiconductor field effect transistor comprising: a silicon-carbide substrate…").

Moreover, nothing in ST's reply or in Dr. Subramanian's rebuttal declaration refutes (because they cannot) the unique properties of SiC that directly impact the design and fabrication of SiC power devices. Instead, Dr. Subramanian claims that such analysis is "beyond the scope of the claims." Dkt. 74-1, ¶ 6. That is simply not true. Because all the disputed terms relate to claims specifically directed to SiC devices, a POSITA's understanding of the key differences between semiconductor devices and the relevant design parameters is critical, especially with respect to ST's indefiniteness claim. *See* Bhat Decl., ¶¶ 6-9. For example, a proper SiC power MOSFET design must successfully address the risk created by the high electric field in the oxide between the gate and the JFET region and the challenges that JFET-region width creates to reach a high blocking voltage. *Id.*, ¶ 6. Thus, designing the right JFET-region width plays an important part when optimizing a high-voltage SiC MOSFET's on-resistance, which is not the case for silicon devices where the oxide on the JFET region is not exposed to such intense electric fields. *Id.*

Thus, ST's absurd arguments concerning the outer boundaries of "less than about three micrometers," which rest on Dr. Subramanian's opinions, only demonstrate that a POSITA must have experience working with and designing SiC semiconductor devices, not just any semiconductor device.

IV. CONCLUSION

For the foregoing reasons, the Court should adopt Purdue's proposed constructions for the disputed terms, and strike Dr. Subramanian's opinions, or alternatively give them little to no weight.

Dated: April 11, 2022

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on April 11, 2022, all counsel of record who have appeared in this case are being served with a copy of the foregoing via the Court's CM/ECF system.

/s/ Mark D. Siegmund
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